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Equivalents:

ABSTRACT:

A real time correlator for correlating a first signal with a second signal comprising a sampler (12, 13) operative to sample first and second input signals, a first store 7, 10 operative to store a plurality N of samples of each of the first and second signals, a main re-circulating store 8 into which a number of samples MIMAGE/FONT

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GB 997198
US 4025772A
US 3670151A
(58) Field of search
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G4A
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(54) Improvements in or Relating to Correlators

(57) A real time correlator for correlating a first signal with a second signal comprising a sampler (12, 13) operative to sample first and second input signals, a first store 7, 10 operative to store a plurality N of samples of each of the first and second signals, a main re-circulating store 8 into which a number of samples M>N of said first signal are fed from the first store, a parallel correlator arrangement 6 in which N samples from the main store are compared in parallel with N samples of the second signal and an integrator 14 responsive to output signals from the parallel correlator for providing an integrated output signal.

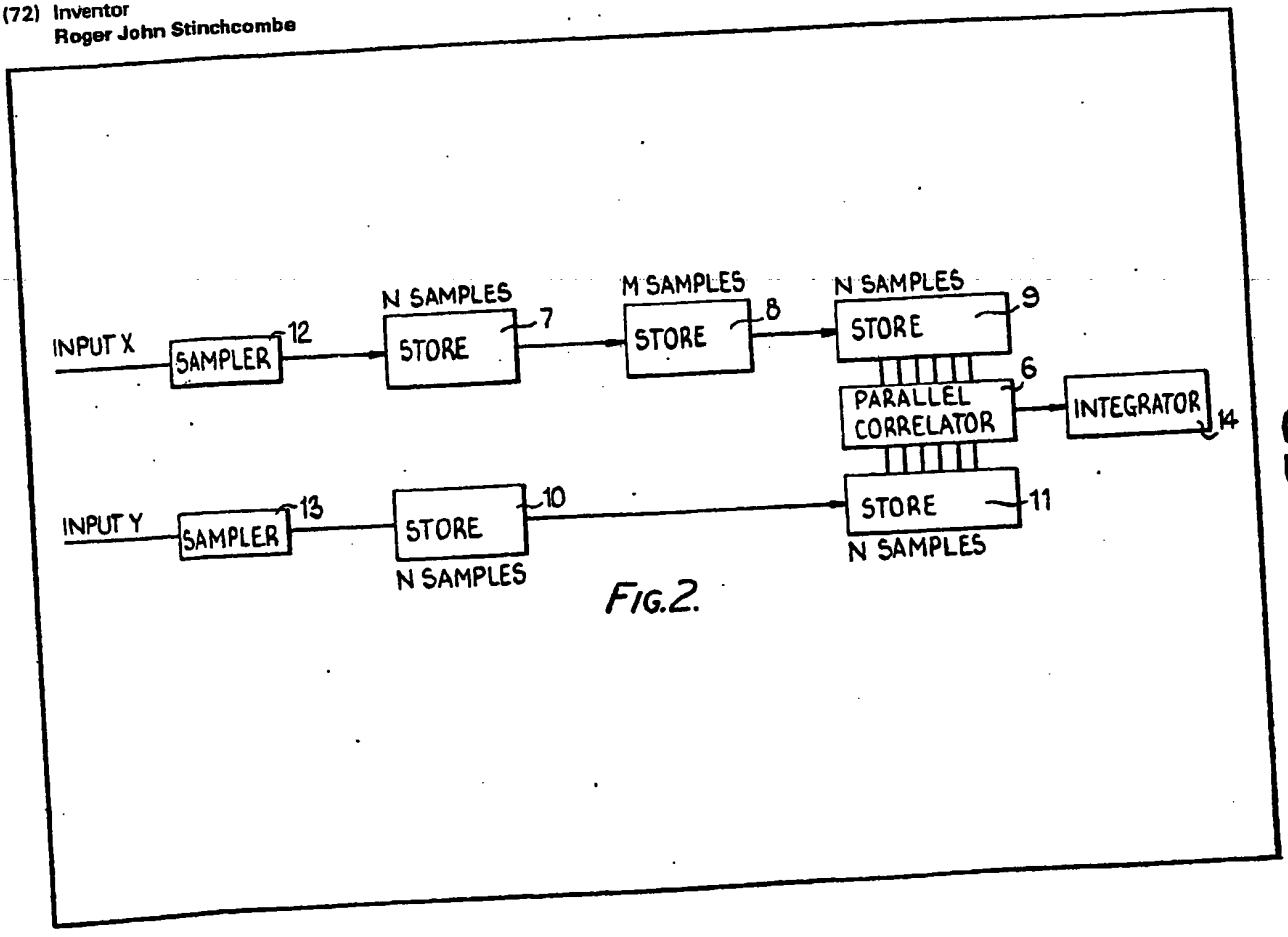

FIG.2.

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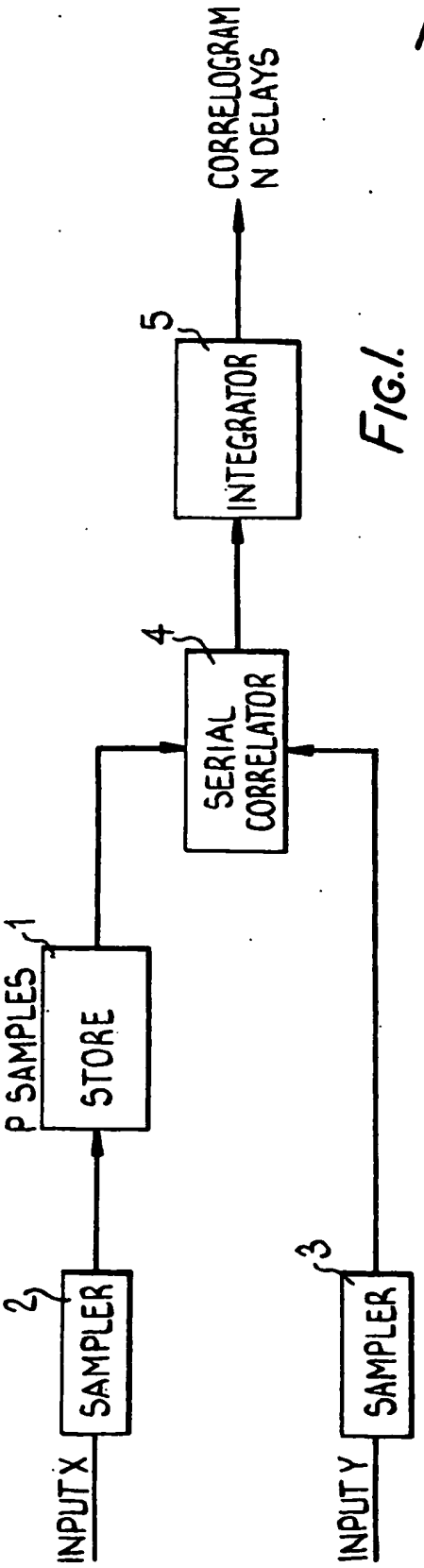
CORRELOGRAM
N DELAYS
5
INTEGRATOR
4
SERIAL
CORRELATOR
P SAMPLES
1
STORE
2
SAMPLER
INPUT X
3
SAMPLER
INPUT Y

FIG.1.

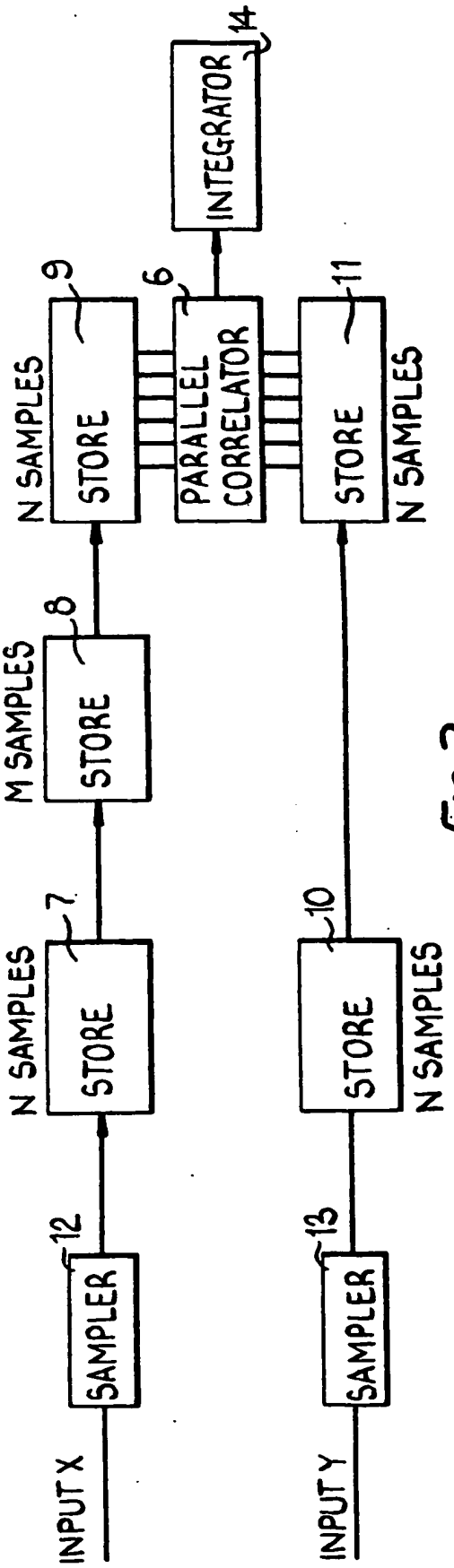
14
INTEGRATOR
9
N SAMPLES
STORE
6
PARALLEL
CORRELATOR
11
STORE
N SAMPLES
8
M SAMPLES
STORE
7
N SAMPLES
STORE
10
STORE
N SAMPLES
12
SAMPLER
INPUT X
13
SAMPLER
INPUT Y

FIG.2.

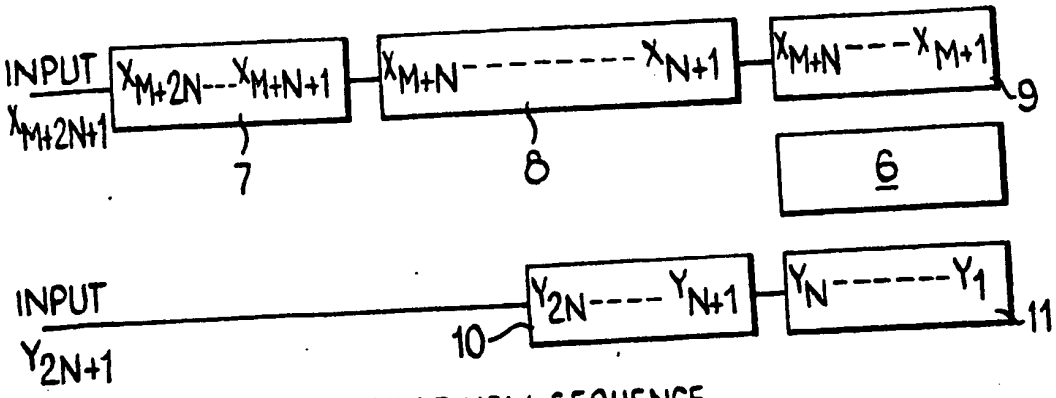

FIG.3(a). START OF NEW SEQUENCE

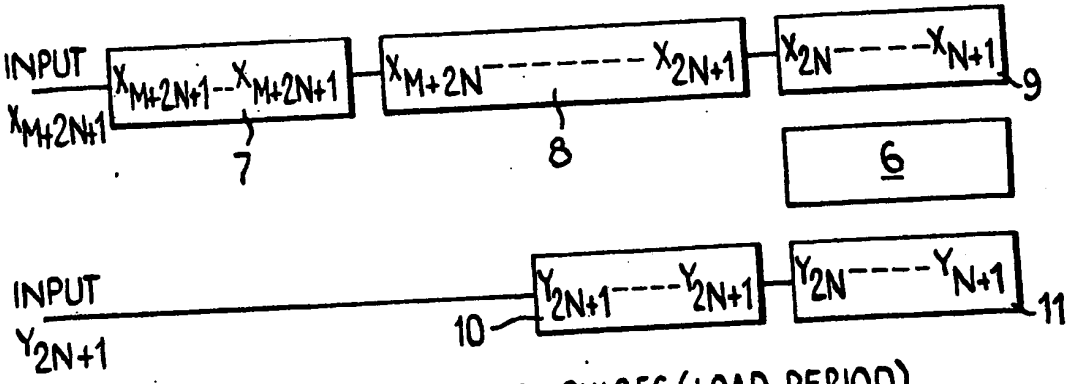

FIG.3(b). AFTER N CLOCK PULSES (LOAD PERIOD)

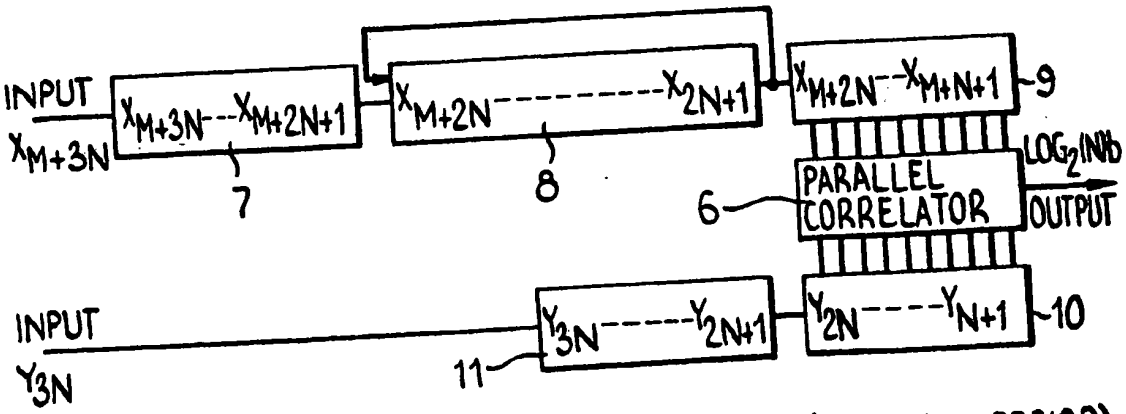

FIG.3(c). AFTER FURTHER M CLOCK PULSES (CORRELATION PERIOD)

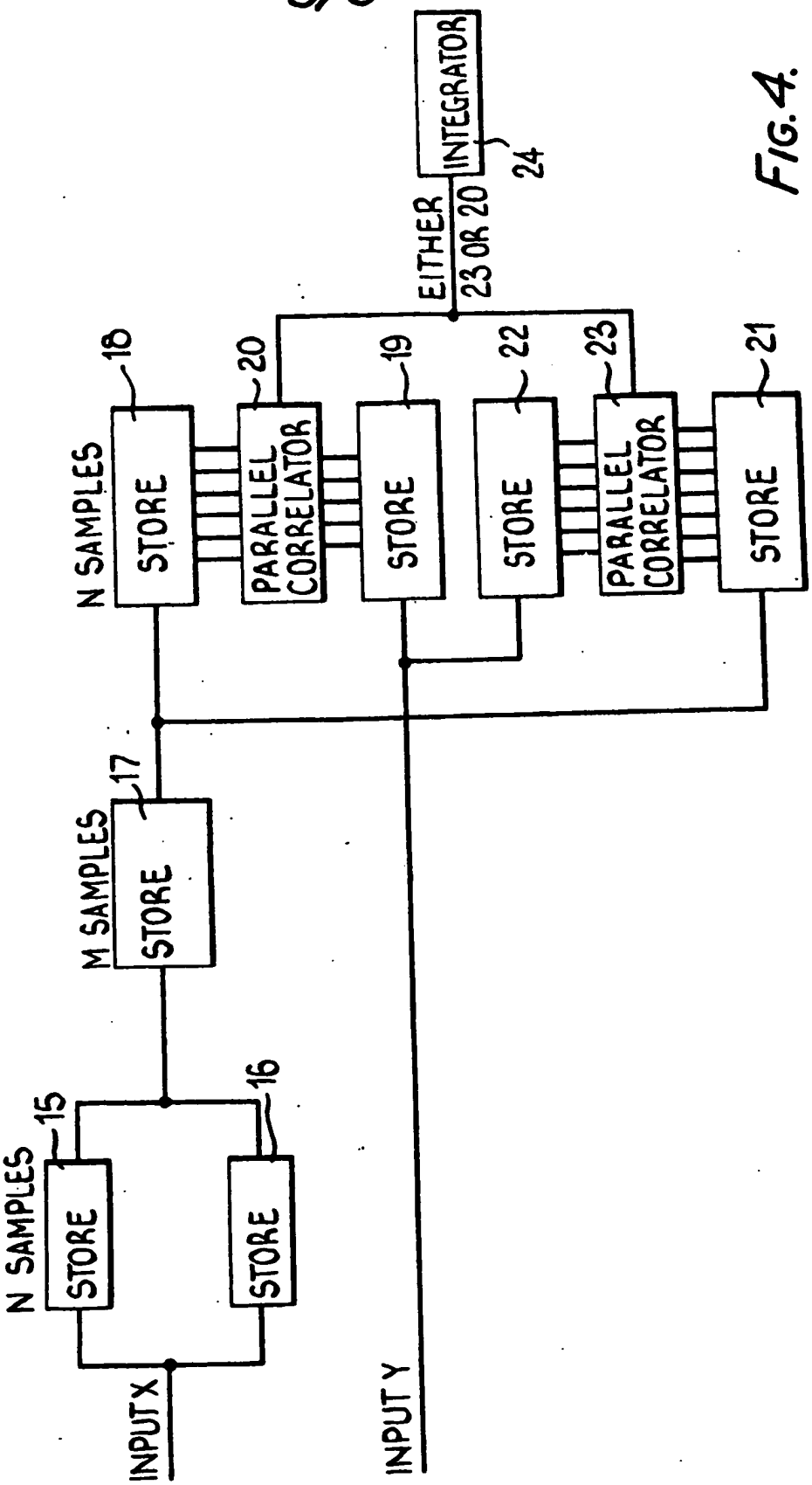
INTEGRATOR
24
EITHER
23 OR 20
18
20
19
22
23
21
N SAMPLES
STORE
PARALLEL CORRELATOR
STORE
STORE
PARALLEL CORRELATOR
STORE
17
M SAMPLES
STORE
15
16
N SAMPLES
STORE
STORE
INPUT X
INPUT Y

FIG. 4.

SPECIFICATION

Improvements in or Relating to Correlators

This invention relates to correlators. The basic deltic correlator is well known but operationally relatively slow. It is an object of the present invention to provide a real time correlator which is faster than the basic deltic correlator.

According to the present invention a correlator for correlating a first signal with a second signal comprises sampling means operative to sample first and second input signals, first storage means operative to store a plurality N of samples of each of said first and second signals, a main re-circulating store into which a number of samples M N of said signal are fed from said first storage means, a parallel correlator arrangement in which samples from the main store are compared in parallel with N samples of the second signal, and an integrator responsive to output signals from the parallel correlator for providing an integrated output signal.

The sampling means may comprise first and second samplers responsive respectively to the said first and second signals.

The first storage means may comprise first and second shift registers responsive respectively to the first and second samplers.

The said parallel correlator arrangement may include a parallel comparator fed in parallel from first and second further stores the said further stores being fed from the first shift register via the said main re-circulating store with samples of the first signal and the said second further store being fed with samples of the second signal from the second shift register, the parallel comparator being arranged to feed the integrator.

In an alternative arrangement the first sampler may be arranged to feed the main re-circulating store via one or other of a pair of stores there being provided two parallel correlator arrangements each responsive to samples of first and second signals.

The correlator arrangements may each comprise a comparator fed in parallel from first and second further stores the main re-circulating store being arranged to feed the first further store of each correlator arrangement, alternately, the second further stores of each correlator arrangement being fed alternately from the sampler responsive to the said second signal, the comparators being arranged alternately to feed the integrator arrangement.

Some exemplary embodiments of the invention will now be described with reference to the accompanying drawings in which:

Figure 1 is a block schematic diagram of a basic simple deltic correlator of a well known type.

Figure 2 is a generally schematic block diagram of a hybrid deltic correlator according to the present invention.

Figure 3a, 3b and 3c are flow charts illustrating operation of the correlator shown in Figure 2 and

Figure 4 is an alternative form of hybrid deltic correlator according to ths present invention.

A basic correlator is well known and is shown in simple form in Figure 1. Referring now to Figure 1 a store 1 holds a number of samples P of an input signal X, the samples being taken by sampler 2 which may take any convenient form. Between each sampling operation the contents of the store 1 is recirculated and each stored sample is multiplied by one sample of an input signal Y taken by a sampler 3, operating at the same rate as the sampler 2 to produce a correlogram of P samples at the output of a serial correlator 4. The serial correlator 4 might comprise an exclusive OR gate so that two similar binary inputs (i.e. 1 and 1 or 0 and 0) produce a binary '1' output and two dissimilar binary inputs (i.e. 1 and 0 or 0 and 1) produce a binary '0' output.

At the start of correlation the store 1 is first filled with P samples. After the store 1 is filled, the next new sample of X is read into the store 1 and the oldest sample is discarded. Hence a new correlogram of P samples can be generated by multiplying by a new sample of Y. This new correlogram consists of the same time delays between samples as the previous one so that it can be integrated with it in an integrator 5 which is conveniently a binary integrator.

The sampling rate of this known system is limited by the speed of reading the store 1 and writing in the new value a re-circulating shift register being used to perform the function of the stores for simplicity. A limit on sampling frequency f_s is then

$$f_s > \frac{f_m}{P+1}$$

where f_m is the speed at which the store can be run.

As shown in Figure 2, in a correlator according to the present invention, a parallel correlator 6 plus an additional store 7 is used instead of the serial correlator of Figure 1 so that the sampling speed may be increased without losing samples.

The method of operation of the arrangement of Figure 2 is similar to the method of operation of the deltic hybrid correlator of Figure 1 except that N sample bits are loaded into main store 8 instead of one bit and these N sample bits are then correlated in parallel, hence producing an integration of N samples for each correlogram delay sample. Thus N clock pulses are used to load N samples of new data whilst there is no correlation, instead of the one clock pulse which in the basic correlator of Figure is used to load one new sample of data between correlation periods. Simple operation is obtained as described above by utilising shift registers in each case to perform the storage function.

The sequence of operation is shown in the flow chart of Figure 3. At the start of the sequence the shift registers 7, 8, 9, 10, 11 contain the samples of X and Y as shown in Figure 3a, the samples taken by the samplers 12 and 13. The shift registers are now shifted at a frequency

$$\frac{M+N}{N}$$

times the sampling frequency f_s so that after N clock pulses (i.e. the load or write period) the registers contain samples of X and Y as shown in Figure 3b, the contents of register 7 having been transferred to register 8 and N samples from register 8 loaded in register 9. Simultaneously, register 11 is loaded from register 10 so that N samples of Y are loaded into the correlator. Register 11 is now held stationary and registers 7 and 10 filled at the sampling frequency with new samples of X respectively from the samplers 12 and 13. Simultaneously, register 8 is clocked at

$$\frac{M+N}{N}$$

times f_s into register 9 and also re-circulated so that after M of these clock pulses the samples of X and Y are as shown in Figure 3C. One sample of the correlogram has thus been output integrated and for N samples and fed into integrator 14 for each of these M clock pulses. The samples of X and Y have now been moved on N samples so that a new sequence can start.

For no missing samples the limit on the sampling frequency has been increased to:

$$f_s \leqslant \left(\frac{N}{M+N}\right) f_m$$

i.e. an increased speed of

$$(P+1) \cdot \left(\frac{N}{M+N}\right)$$

Assuming P=M for the same length correlogram this is

$$\frac{(M+1)N}{(M+N)}$$

which is approximately equal to N for M N, or approximately N times as fast. The speed can be slightly increased over that explained above by using switches, extra stores for shift register 7 and incorporating shift register 10 into a double parallel correlator system as shown in Figure 4.

Referring now to Figure 4, shift registers 15 and 16 are used to store the new samples of input X whilst correlation is being performed. Shift register 17 is shifted at

$$\left(\frac{M+N}{N}\right)$$

time the sampling frequency and fed into shift register 18. Simultaneously shift register 15 is fed into shift register 17. After N samples have been taken shift register 17 is recirculated so that a new set of M samples are kept in register 17 and M+N samples pass through the shift register 18. These are then correlated with N samples of input Y held in the shift register 19, to produce a correlogram of M+N delays integrated for N samples. While the output is being taken out of parallel correlator 20 the samples of input X are being fed into the shift register 16 and the samples of the input signal Y into register 21. Thus after

$$\frac{N}{f_s}$$

seconds the register 15 may be used instead of the register 16 and in the same way the shift register 21 will be used instead of the shift register 18 and the shift register 22 will be used instead of the shift register 19. If the shift register 22 is then held stationary, the next set of correlogram points will be obtained from the parallel correlator 23. These can be integrated with the previous set from parallel correlator 20. The set are fed to integrator 24. For no missing samples the limit on the sampling frequency has been increased to

$$f_s \leqslant \left(\frac{N}{M+N}\right) f_m$$

where P M+N
i.e. an increase in speed of

$$\frac{(M+N+1)(N)}{(M+N} \simeq N \text{ for } M \gg N$$

A simple way of considering this option is that the load time of the first hybrid processor has been removed by using more store and processing. Note that again that the shift register may be serial registers or random access memories.

Claims

1. A Correlator for correlating a first signal with a second signal comprising sampling means operative to sample first and second input signals, first storage means operative to store a plurality N samples of each of said first and second signals, a main re-circulating store into which a number of samples M N of said first signal are fed from said first storage means, a correlator arrangement in which samples from the said main store are compared in parallel with N samples of the second signal, and an integrator responsive to output signals from the said correlation arrangement for providing an integrated output signal.

2. A correlator as claimed in claim 1 wherein the sampling means comprises first and second

samplers responsive respectively to the said first and second signals.

3. A correlator as claimed in claim 2 wherein the first storage means comprises first and second shift registers responsive respectively the first and second samplers.

4. A correlator as claimed in claim 3 wherein the said correlator arrangement includes a parallel comparator fed in parallel from the first and second further stores, the further stores being fed from the first shift register via the said main re-circulating store with samples of the first signal and the said second further store being fed with samples of the second signal from the second shft register, the parallel comparator being arranged to feed the integrator.

5. A correlator as claimed in claim 2 wherein the first sampler may be arranged to feed the main re-circulating store via one or other of a pair of stores, there being provided two parallel correlator arrangements each responsive to samples of first and second signals.

6. A correlator as claimed in claim 5 wherein the correlator arrangements each comprise a comparator fed in parallel from first and second further stores the main re-circulating store being arranged to feed the first further store of each correlator arrangement alternatively, the second further stores of each correlator arrangement being fed alternately from the sampler responsive to the said second signal, the comparators being arranged to feed the integrator arrangement.

7. A correlator substantially as hereinbefore described with reference to the accompanying drawings.

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